Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

1. (currently amended) A method of testing a semiconductor wafer, the semiconductor wafer having a plurality of die that contain static random access memory (SRAM) arrays, comprising the steps of:

   (a) coupling an array of probes to the semiconductor wafer; ~~and thereafter~~

   (b) applying a voltage difference across ~~a plurality of adjacent bitline pairs and/or worldine pairs~~ a pair of closely spaced wordlines or bitlines of one or more static random access memory (SRAM) arrays ~~of at least one die of the semiconductor wafer~~, wherein the voltage difference across the pair of closely spaced wordlines or bitlines exceeds a voltage difference that the wordlines or bitlines would experience in normal operation; ~~the voltage being larger than an operational supply voltage for~~ of ~~the one or more SRAM arrays, to thereby induce failure of metal stringers or defect;~~ and

   (c) identifying whether electrical shorting occurs across said pair of closely spaced wordlines or bitlines.

2. (currently amended) The method of claim 1, further comprising the step of simultaneously applying the voltage difference across respective pairs of

substantially all parallel bitline pairs and/or wordline pairs of the one or more SRAM arrays.

3. (currently amended) The method of claim 1, further comprising the step of simultaneously applying a voltage across respective pairs of substantially all parallel bitline pairs and/or wordlines pairs of the one or more SRAM arrays of more thatn one die of the semiconductor wafer.

4. (currently amended) The method of claim 1, further comprising the step of applying the voltage difference across other adjacent, parallel metal lines of the one or more SRAM arrays.

5. (currently amended) The method of claim 1, further comprising the step of applying the voltage difference at a magnitude of equal to or greater than two times the operational supply voltage.

6. (currently amended) The method of claim 2, further comprising the step of applying the voltage difference at a magnitude of equal to or greater than two times the operational supply voltage.

7. (currently amended) The method of claim 3, further comprising the step of applying the voltage difference at a magnitude of equal to or greater than two times the operational supply voltage.

8. (currently amended) The method of claim 4, further comprising the step of applying the voltage difference at a magnitude of equal to or greater than two times the operational supply voltage.

9. (currently amended) The method of claim 1, further comprising the step of prerforming step b at an elevated temperature.

10. (currently amended) The method of claim 9, further comprising the step of applying the voltage difference at a magnitude of equal to or greater than two times the operational supply voltage.

11. (currently amended) The method of claim 3, further comprising the step of prerforming step b at an elevated temperature.

12. (currently amended) The method of claim 4, further comprising the step of prerforming step b at an elevated temperature.

13. (currently amended) A semiconductor wafer having one or more die with a static random access memory (SRAM) array integrated therein, comprising:

a test circuit integrated with the SRAM array; and

connections that couple said test circuit to the SRAM array;

wherein during probing, said test circuit applies a voltage difference across a plurality of adjacent bitline pairs and/or worldine pairs of the SRAM array, the voltage difference being larger than an operational supply voltage for the SRAM array, to identify whether electrical shorting occurs across one or more of said plurality of adjacent bitline pairs and/or wordline pairs.~~, to thereby induce failure of metal stringers or defects.~~

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-13 are pending in the application, with 1 and 13 being the independent claims. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

In the May 22, 2003 Office Action, Claim 13 was rejected as being anticipated by Mo et al., U.S. Patent No. 5,956,279 ("Mo patent"). Applicants respectfully traverse this rejection. Based on the remarks set forth below, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The Mo patent discloses a testing circuit to cycle memory cells by providing a current to word or bit lines connected to the memory cells. The Mo patent discloses a testing circuit that provides sufficient current to drive multiple word or bit lines to exercise memory cells. The Mo patent does not disclose that different voltages are applied across adjacent word or bit lines. Nor, does the Mo patent disclose that voltages across adjacent word or bit lines will be greater than typical operational levels.

As such, the Mo patent does not disclose a test circuit that applies a voltage difference across a plurality of adjacent bitline pairs and/or worldine pairs of the SRAM array, the voltage difference being larger than an operational supply voltage for the SRAM array, to identify whether electrical shorting occurs across one or more of said plurality of adjacent bitline pairs and/or wordline pairs, as is disclosed in claim 13, as amended herein.

Thus, Applicants respectfully submit that the Mo patent does not disclose, teach, or suggest each and every element in claim 13. A claim is anticipated only if each and every element set forth in the claim is found in a single prior art reference. MPEP § 2131. For at least the reasons stated above, claim 13 is patentable over the Mo patent. Applicants respectfully request that the Examiner reconsider and withdraw the rejection of claim 13.

Rejections under 35 U.S.C. § 103

In the May 22, 2003 Office Action, the Examiner rejected claims 1-8 as being unpatentable under 35 U.S. C. § 103(a) as being unpatentable over Mo et al., U.S. Patent No. 5,956,279 ("Mo patent"). Applicants respectfully traverse this rejection. Based on the remarks set forth below, Applicants respectfully request that this rejection be reconsidered and withdrawn.

As amended herein, claim 1 discloses applying a voltage difference across a pair of closely spaced wordlines or bitlines of one or more static random access memory (SRAM) arrays, wherein the voltage difference across the pair of closely spaced

wordlines or bitlines exceeds a voltage difference that the wordlines or bitlines would experience in normal operation. The Mo patent does not disclose, teach or suggest this element.

Furthermore, as amended herein, claim 1 discloses the step of identifying whether electrical shorting occurs across said pair of closely spaced wordlines or bitlines. The Mo patent does not disclose, teach or suggest this element either. In fact, as discussed in Applicant's previous Amendment and Reply, dated March 20, 2003, the Mo patent teaches away from the present invention by suggesting that adjacent bit and word lines will be at the same voltage level.

Applicants respectfully submit that the Mo patent does not suggest each and every element in claim 1. In fact, the Mo patent presents a method that teaches away from the present invention. For at least the reasons stated above, claim 1 is patentable over the Mo patent. Applicants respectfully request that the Examiner reconsider and withdraw the rejection of claim 1.

Because each dependent claim incorporates all of the elements of the independent claim from which it depends, as well as additional features, claims 2-8, which depend upon claim 1 are also patentable over the Mo patent.

In the May 22, 2003 Office Action, the Examiner rejected claims 9-12 as being unpatentable under 35 U.S. C. § 103(a) as being unpatentable over Mo et al., U.S. Patent No. 5,956,279 ("Mo patent") in view of McClure, U.S. Patent No. 5,619,462 ("McClure patent"). Applicants respectfully traverse this rejection. Based on the remarks set forth below, Applicants respectfully request that this rejection be reconsidered and withdrawn.

In rejecting these claims, the Examiner has relied upon the Mo patent to support the position that claim 1 is not patentable over the Mo patent. The Examiner relies upon the McClure patent to support the position that the step of performing step b at an elevated temperature is disclosed in the McClure patent. As shown above, claim 1 is non-obvious and patentable over the Mo patent. Moreover, the McClure patent fails to teach or suggest the above-described shortcomings of the Mo patent. Since each of claim 9-12 depends on claim 1, and because each dependent claim incorporates all of the elements of the independent claim from which it depends, as well as additional features, claims 9-12 are also patentable over the prior art of record for at least the above described reasons. Applicants respectfully traverse this rejection. Applicants respectfully request that this rejection be reconsidered and withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Preliminary Amendment is respectfully requested.

Respectfully submitted,

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